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Finding

In the last decade or so, the MOSFETS's have played a crucial role in enhancing the circuit performance and other parameters, owing to the downscaling of device dimensions. The device scaling trend, which was predicted long back by Gordon Moore, has been followed till now but cannot be continued further on these devices due to scaling issues like Short Channel Effects. The semiconductor industry is struggling to maintain this downscaling trend, as MOS power consumption cannot get reduced accordingly. So, further implementation of Moore's law on silicon-based devices is unachievable as problem of power crisis arises in silicon-based MOS transistors. The carrier transport mechanism in a MOSFET is the reason behind increased power consumption when device scaling is continued.

The MOSFET's work on the principle of thermionic emission of electrons, which restricts the subthreshold slope to a fixed value of 60mV/decade. This constant value of subthreshold slope with continued voltage scaling leads to increased power dissipation, as off-current increases proportionally with decreased supply voltage. Therefore, a need for devices which can perform better at minimal input supply arises, hence raising the importance of device scaling and power supply reduction. This requirement cannot be met with traditional silicon based MOSFET's, hence the need to look for MOSFET alternatives.

The solution to the limitations faced by silicon-based MOS devices is to find new materials with improved performance that could be used in place of silicon and to look for novel device architectures that are based on a different transport mechanism. The devices which are not subjected to SS limitation and have a steeper slope are known as 'Steep-Slope Devices'. Steep SS devices are considered as the best alternative to the conventional MOSFET. One such device is a Tunnel Field Effect Transistor, commonly referred to as TFET. The subthreshold slope limitation of a MOSFET is overcome in this device because the carrier transport mechanism is based on Band-To-Band-Tunneling (BTBT) in which band bending takes place at the tunneling junction, on application of appropriate voltage at the gate terminal of the device.

The work carried out in this thesis is designing, simulation and investigation of various TFET architectures so as to improve the TFET on-current, decrease the off-current, decrease ambipolarity and improve SS. The enhancement of DC parameters as well as improvements in RF performance has also been investigated.