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Topic of Research: Design and Simulation of Multi-Gate Transistors for Low Power and High Performance Applications

Findings

The thesis discusses the design and simulation of multi-gate transistors for low power and high-performance applications. The shortcomings of conventional transistors are discussed in detail. Due to scaling down of the transistors, SCEs come into picture, so elaborated extensively. Junctionless transistors are explored in detail as a solution of the difficulties encountered by conventional CMOS technology. The advantages and the disadvantages of each proposed device are indicated. The proposed designs are compared with the previously published devices. This work is explained in different chapters and their brief overview is given below:

Chapter one provides a comprehensive introduction to several junctionless transistors that have been extensively studied and documented in the literature. A comprehensive analysis is provided on junctionless transistors utilizing BULK, SOI, and SELBOX technology. Subsequently, in this chapter, objectives are determined and presented through an analysis of existing material and research.

In the second chapter, Junctionless FinFET on SELBOX technology has been proposed. Using simulation studies, the structural and operational features of a junctionless FinFET based on SOI and a FinFET based on selective buried oxide (SELBOX) were evaluated for gate lengths of 15 nm and beyond. Independently adjusting factors like buried oxide thickness, substrate doping, substrate bias, and the spacing between buried oxide layers can further improve the characteristics of the SELBOX FinFET.

In third chapter, an evaluation is performed to determine the effects of uniform and non-uniform doping on the results produced by SOI and SELBOX FinFET devices with a gate length below 7 nm. The simulations are done on SILVACO TCAD. The analysis and

comparison of the performance of uniformly doped SOI and SELBOX transistors are performed. In addition, an analysis and comparison are done for SOI and SELBOX FinFETs with non-uniform doping.

Chapter four provides an explanation of the SELBOX FinFET with PGP (Partial Ground Plane), which is doped both uniformly and non-uniformly. First, we compare the performance of a SELBOX Transistor that is uniformly doped without PGP to a SELBOX Transistor that is uniformly doped with PGP. Then, we study and compare the performance characteristics of a SELBOX Transistor that is non-uniformly doped with PGP to the approach without using PGP.

The analysis and comparison of Analog/RF performance of the uniformly and non-uniformly doped SELBOX FinFET and SOI FinFET are performed in chapter five. The SELBOX transistor, which has a uniform doping profile, is being compared to a uniformly doped SOI transistor. Non-uniformly doped SELBOX FinFET is compared to non-uniformly doped SOI FinFET.

Chapter 6 involves doing numerical simulations on the SOI-JL FinFET with buried Metal-Fin and P-Fin. The BMF structure employs Schottky junction-induced depletion, which enhances gate control and improves its performance. We have performed an analysis and comparison of both devices based on parameters such as DIBL, SS, I_{ON}/I_{OFF} ratio, and threshold voltage. SOI-JL FinFET with buried Metal-Fin is superior to that of SOI-JL FinFET with buried P-Fin.

In chapter 7, summary of the thesis is given. It also contains the works that can be performed in future.