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Findings

Over the past few decades, continuous transistor miniaturization has led to increased transistor density but also significantly surging overall power consumption per chip. Moreover, simultaneously increasing both transistor density and operating frequency has become unfeasible. To address this, Moore's Law has been maintained by increasing transistor counts while capping microprocessor frequencies at a few GHz. To lower the power consumption, dynamic power consumption ($P_{Dynamic}$) can be quadratically reduced by lowering the supply voltage (V_{DD}) in power-constrained applications. However, scaling V_{DD} below 0.8 V has proven extremely challenging in MOSFET. Achieving lower V_{DD} while maintaining high performance requires reducing the threshold voltage (V_{TH}), but this exponentially increases static leakage power consumption ($P_{Leakage}$) due to the exponential rise in OFF-state leakage current (I_{OFF}) caused by the thermal energy-limited *Boltzmann tyranny*, which limits the subthreshold swing (SS) of conventional MOSFET to 60 mV/dec during ON-to-OFF transitions. Consequently, reducing static power consumption has become a significant challenge. Reducing SS below 60 mV/decade in MOSFETs is thermodynamically impossible, even without short-channel effects (SCEs). Moreover, lowering V_{TH} leads to higher static power consumption, making MOSFETs unsuitable for ultra-low-power applications ($V_{DD}< 0.4$ V).

Therefore, achieving lower V_{TH} without increasing I_{OFF} requires devices based on novel physical principles and carrier injection mechanisms beyond the thermionic emission used in traditional MOSFETs. For this, a much steeper slope switch would lower V_{TH} without increasing I_{OFF}, unlike conventional MOSFETs. This can be achieved by employing quantum mechanical band-to-band tunneling, as in Tunnel FETs (TFETs), or by implementing negative capacitance (NC) through ferroelectric gate oxides, as seen in NCFETs. Alternatively, lowering the temperature below 300 K to deep cryogenic temperature levels would also allow SS to be reduced in MOSFETs while maintaining the thermionic emission mechanism. This thesis explores all these possibilities to enhance the performance with lowered SS values for ultra-low power by proposing various novel point and line tunneling FET architectures, introducing novel NC-based line TFET designs, and analyzing ultra-scaled MOSFETs at deep cryogenic temperatures to achieve improved SS performance. Through rigorous TCAD simulation and NEGF simulation, the proposed designs are thoroughly explored and analyzed, offering promising solutions for future low-power technologies.