Name of the Ph.D. Scholar: SUNIL KUMAR
Name of the Ph.D. Supervisor: Dr. SAJAD A. LOAN
Name of the Department: Electronics & Communication Engineering
Title of the Thesis: Design and simulation of Novel Nano SOI based Engineering Devices for Nano electronics applications.

ABSTRACT

Silicon, one of the Nature's biggest gift has been serving us from the last many decades in various forms of silicon semiconductor devices and silicon integrated circuits (IC). Silicon has some unique and important properties and advantages, one of the important advantages is its abundance in nature. This is the reason that the silicon devices are comparatively cheap and more than 90% electronics devices are from silicon only. The silicon MOSFET and silicon based CMOS circuitry are the backbone of current electronic industry. The continuous and successful scaling of silicon MOS devices is indeed responsible for keeping Moore's law valid and alive till date. It is scaling of MOSFET device dimensions which has fulfilled the Richard Feynman dream of storing entire encyclopaedia Britannia on the tip of a pin. Presently, we are in a position to store many encyclopaedias in a very very small chip area. The scaling has indeed enhanced the overall performance of IC technology; enhanced processing speed, reduced power consumption, increased functionality etc. Indeed, tera-scale integrations, realization of ICs with billions of transistors is attributed to the successful scaling of MOSFET device dimensions. Now the semiconductor scientists, engineers and researchers ask two important questions to visionaries "*How long will the silicon MOS technology go? And what will happen after it? Do we have some alternative material/device in place, which can replace silicon/CMOS technology efficiently*?"

The fact of the matter is that the era of silicon device technology is nearing its end and the further scaling of MOS devices below 22/18 nm is extremely difficult due severe SCEs, increase in static power dissipation, gate oxide tunnelling and a severe increase in source /drain series resistances in a nanoscaled devices etc. There is an immediate need to address these problems in nanoscaled devices to keep Moore's law valid and alive. The various solutions have been provided by the researchers. The replacement of silicon by other materials like SiGe, GaAs, GaN etc. and the replacement of MOSFET by other device structures, like multigate structures, carbon nanotube (CNT) FET, FinFETs etc are some of the solutions. However, the solutions are complex and costly, particularly the replacement of silicon by other materials.

In this thesis work, we tried to address the above mentioned problems by providing solutions which still use silicon as a basic material for fabrication and hence retain all the advantages of silicon technology. Our solutions does not demand the scaling of device dimensions to extract more and more performance out of the devices and to face the severe scaling issues. We designated and simulated devices which realize circuit, gate and blocks directly at the device level. Herein, a single transistor directly realizes a gate action, which normally is being realized by multiple transistors in the conventional technology. A combination of just two gate engineered transistors directly implements a Boolean equations which can be realized by dozens of transistors. A metallic source/drain based Sajad-Sunil-Schottky (SSS) device is proposed and simulated. This device realize directly an inverter and its modified version

realizes a transmission gate. The combination of SSS based inverter and SSS based TG has been used to realize many combinational circuits. A hybrid doped MOSFET is proposed and simulated, with significantly improved short channel effects suppression capability without a substantial area increase. Further, patterned gate device technology directly implements a Boolean equation of any size.

The work done in this thesis is divided into eight chapters, the details are given below.

Chapter 1 gives the general background of the work done in this thesis. The motivation behind this work is also is given. The various problems which the state of the art nanoscaled devices face are also discussed briefly. Further, this chapter discusses various design tools and simulators used in designing various proposed and conventional devices.

In chapter 2, the state of the art literature related to nanoscaled devices particularity, the Schottky barrier MOSFET is reviewed. The various issues which the nanoscaled devices face are elaborated. The electrically induced doping based devices are also reviewed in this chapter.

In chapter 3, a novel structure of a metal source/drain Schottky MOSFET is proposed and simulated. A complete study of the proposed device, known as the Sajad-Sunil-Schottky (SSS), has been done. The SSS device is a multifunctional device and can realize n-transistor, p-transistor and an inverter action directly.

In chapter 4, a novel structure of a transmission gate employing the SSS device is designed and simulated. A complete study of the proposed transmission gate device has been done. In this device, n-channel and p-channel turn ON or OFF simultaneously to realize a transmission gate action

Chapter 5 discusses the application part of the SSS technology. The SSS technology has been used to realize universal gates and other combinational circuits in this chapter. A comparative analysis is being made between the proposed technology based gates and the conventional technology based gates.

Chapter 6 discusses a novel structure of a nanoscaled multifunctional device employing hybrid doping concept. Again a NAND gate and a NOR gate action is being realized at the device level of abstraction.

In chapter 7, the concept of gate electrode engineering has been used to realize multifunctional devices. Using this novel approach a Boolean equation of any size can be implemented by just two gate engineered transistors. Various examples have been discussed in this chapter.

Chapter 8 concludes the thesis work. It highlights various issues addressed in this thesis and gives the direction for the future work.