PhD RESEARCH FINDINGS

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PhD Topic: "**Design and Simulation of Green Nanoelectronics Devices**"

PhD Research Findings:

This thesis is centered around designing and investigating high performance TFET, which can enable V_{DD} reduction without compromising the ON-state performance, and keep the Moore's law valid and alive. The 2D-TCAD simulation methodology has been used for the design and investigation at device and circuit level. The finding of the research has been briefly summarized in the following points.

- A new TFET architecture with orthogonal gate control have been proposed and simulated. The device exhibits much improved parasitic leakage, suppressed ambipolar leakage, and simultaneously double the ON-state current. The model parameters used in simulations were calibrated before carrying on the study. Several variations of device structure are introduced initially and compared to arrive at a final structure with optimized device dimensions. It is found that the proposed device outperforms the DG architecture based TFET due to orthogonally controllable silicon film and oxide thicknesses.

- We simulated a DG architecture based TFET structure that is drain engineered. This enables us to minimize the sharpness of tunnel junction at the drain, thus, widening the barrier width. At the same time, higher channel doping at the source junction increases the electric field and thus lower the tunnel barrier width.

- We have proposed a GAA architecture with a low WF metal with negative electron Schottky-barrier height (SBH) as a drain. This minimizes the lateral BTBT (L-BTBT) considerably. L-BTBT is the movement of carriers (holes) from the drain conduction band (CB) into the channel valence band (VB) during the OFF state. Impact of varying WF at channel-drain junction on the device characteristics is studied. It is observed that SBH 6 eV is required to mitigate L-BTBT compared to the conventionally-doped and junctionless (JL) NW counterpart.

- We have proposed surface potential and subthreshold current models for a buried-metal-layer based junction-less transistor, for the first time, and the proposed models are verified with the simulation results. The scalability of the BML technology is benchmarked against the existing DG architecture, using its natural length (λ), electrostatic integrity (EI), Vth roll-off and SS as the figure of merits.